

Introduction

This document describes the operation and use of a test bitstream for the DDR interface on the LatticeEC™ Advanced Evaluation Board and the LatticeXP Advanced Evaluation Board. This design implements a DDR memory test logic to test the SO-DIMM DDR memory module when it's installed on the evaluation board. The maximum frequency of this design is targeted to 200MHz for the LFEC20E-5 and 167MHz for the LFXP10C-5.

Lattice recommends the use of one of the following DDR memory modules for use with the LatticeEC and LatticeXP Advanced Evaluation Boards:

- Micron: MT8VDDT3264HDG-40BF4
- Corsair: VS512SDS400
- PQI: MD4212UOE

The bitstream described in this document was developed using the Lattice DDR SDRAM Controller - Pipelined for LatticeECP™ and LatticeEC IP core. (DDRCT-GEN-E2-N1). More information on this IP core can be found on the Lattice web site at: www.latticesemi.com/ip.

Both the LatticeEC Advanced Evaluation Board and the LatticeXP Advanced Evaluation Board feature a 200-pin SO-DIMM DDR memory socket. See the user's manual of the appropriate board for further information on this socket.

Three LatticeEC bitstream files are included in the ZIP file for the support of the following standards:

- ddr_verilog_pnr_133MHz_DDR266.bit
ddr_vhdl_pnr_133MHz_DDR266.bit
- 166MHz DDR333
ddr_verilog_pnr_166MHz_DDR333.bit
ddr_vhdl_pnr_166MHz_DDR333.bit
- 200MHz DDR400
ddr_verilog_pnr_200MHz_DDR400.bit
ddr_vhdl_pnr_200MHz_DDR400.bit

Two LatticeXP JEDEC files are included in the ZIP file for the support of the following standards:

- 133MHz DDR266
ddr_verilog_pnr_133MHz_DDR266.jed
ddr_vhdl_pnr_133MHz_DDR266.jed
- 166MHz DDR333
ddr_verilog_pnr_166MHz_DDR333.jed
ddr_vhdl_pnr_166MHz_DDR333.jed

Limitations

The 200-pin SO-DIMM DDR module contains a 64-bit wide data bus. However, in order to reserve I/Os for demonstrating other features on the evaluation board only 16 data bits are connected to LFEC20E or LFXP10C FPGA.

This design uses the evaluation version of the Lattice IP core. The configuration is limited to a 12-bit row address, a 9-bit column address and one chip select (rank).

Board Setup

For the LatticeEC Advanced Evaluation Board:

1. Set the V_{CCIO} pins of all banks to 2.5V by putting all eight jumpers of JP2-JP5 to JP4.
2. Push SW4 down.
3. Set all three pins (CFG2, CFG1, CFG0) of SW5 ON. (Push all SW5 pins down.)
4. SW1 pin 1 is the “rst_n” reset signal. This needs to be pulled up to exit the reset state.
5. (Rev-C PCB and later only): Located on the 3-pin header between SW4 and SW5. If you are running 200MHz/DDR400, select 2.6V by moving jumper to the upper two pins. For 133MHz/DDR266 and 166MHz /DDR333, select 2.5V.
6. The 33.33MHz oscillator must be installed in pins 2, 8 (GND), 9 (CLK) and 15 (3.3V) of the DIP-16 socket. This will provide a clock signal to the FPGA through ball F6.
7. Install the SO-DIMM DDR memory module.
8. Use a 5V power supply that can provide adequate current to the board.

For the LatticeXP Advanced Evaluation Board:

1. Set the V_{CCIO} pins of banks 0, 1, 6, 7 to 2.5V by moving all jumpers from JP1, JP2 or JP4 to JP3.
2. Install four jumpers on either JP7, JP9, or JP11 to select the core voltage for LFXP10C.
3. Set the pins (CFG1, CFG0) of SW4 OFF (pull the SW4 pins up).
4. SW1 pin 8 is the “rst_n” reset signal. This needs to be pulled up to exit the reset state.
5. Enable the power circuit by installing a jumper between pins 2 and 3 of JP15-JP18. Pins 2 and 3 of JP15 and JP16 are the two left-hand pins. Pins 2 and 3 of JP17 and JP18 are the lower two pins.
6. The 33.33MHz oscillator must be installed in pins 1, 7 (GND), 10 (CLK) and 16 (3.3V) of the DIP-16 socket. This provides a clock signal to the FPGA through ball A10.
7. Install the SO-DIMM DDR memory module
8. Use a 5V power supply that can provide adequate current to the board.

Steps for Programming Bit Files into SPI Serial Flash

The following steps are for the LatticeEC Advanced Evaluation Board only:

1. Connect your PC to the target board using a Lattice ispDOWNLOAD® Cable
2. Launch the ispVM® System software
3. Click **File -> New**
4. Click **Edit -> Add Device**
5. Click **Select** and select **FPGA Loader** for “Device Family” and then click **OK**
6. Highlight **Configuration Data Setup** and click the lower **Browse** to select either **ddr_test_200MHz_DDR400.bit**, **ddr_test_166MHz_DDR333.bit**, or **ddr_test_133MHz_DDR266.bit**
7. Highlight **Flash Device** and click **Select...** to select **SPI Serial Flash, SPI-M25P80, 8-pin SOIC**, then click **OK**
8. Click **OK** again to close the FPGA Loader window

9. Make sure the SW4 switch is in the **UP** position and the download cable is connected to either JP6 or JP8.
10. Click **GO** to program bit to SPI flash.
11. Push SW4 back to the **DOWN** position.

Memory Testing Algorithm

This test is completed by writing test_data into the address space of the user interface (from 0 to 7FFFFC), then reading the data back to check for errors.

The test starts by writing 0x01 to byte_1 (D15-D8) and 0xfe to byte_0 (D7-D0) of address 0x00000. The test data is then rotated within the byte and the address is increased by four for the next write cycles.

When the write reaches address 0x7fff, reading and verification will begin, starting at address 0x00000, then address 0x00004, etc. (see below)

After the read reaches address 0x7fff, one test cycle is considered as complete. The test_data will then be changed for the next test.

In order to prevent writing the same pattern to the same address location for every test, the test_data is rotated and then inverted at address 0x00000 before a new test starts.

The testing sequences are as follows:

	byte_1 D15-D8	byte_0 D7-D0
Test 1 started-----		
Write to address 0x00000:	0x01	0xfe
Write to address 0x00004:	0x02	0xfd
Write to address 0x00008:	0x04	0xfb
Write to address 0x0000c:	0x08	0xf7
Write to address 0x00010:	0x10	0xef
Write to address 0x00014:	0x20	0xdf
Write to address 0x00018:	0x40	0xbf
Write to address 0x0001c:	0x80	0x7f
Write to address 0x00020:	0x01	0xfe
Write to address 0x00024:	0x02	0xfd
Write to address 0x00028:	0x04	0xfb
Write to address 0x0002c:	0x08	0xf7
:		
:		
Write to address 0x7fff:	0x80	0x7f
Read from address 0x00000		
Read from address 0x00004		
:		
:		
Read from address 0x7fff		
Test 2 started-----		
Write to address 0x00000:	0xfd	0x02
Write to address 0x00004:	0xfb	0x04
Write to address 0x00008:	0xf7	0x08
Write to address 0x0000c:	0xef	0x10
Write to address 0x00010:	0xdf	0x20
Write to address 0x00014:	0xbf	0x40

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Write to address 0x00018: 0x7f 0x80
Write to address 0x0001c: 0xfe 0x01
Write to address 0x00020: 0xfd 0x02
Write to address 0x00024: 0xfb 0x04
Write to address 0x00028: 0xf7 0x08
Write to address 0x0002c: 0xef 0x10
:
:
Write to address 0x7fff: 0xfe 0x01
Read from address 0x00000
Read from address 0x00004
:
:
Read from address 0x7fff

```

```

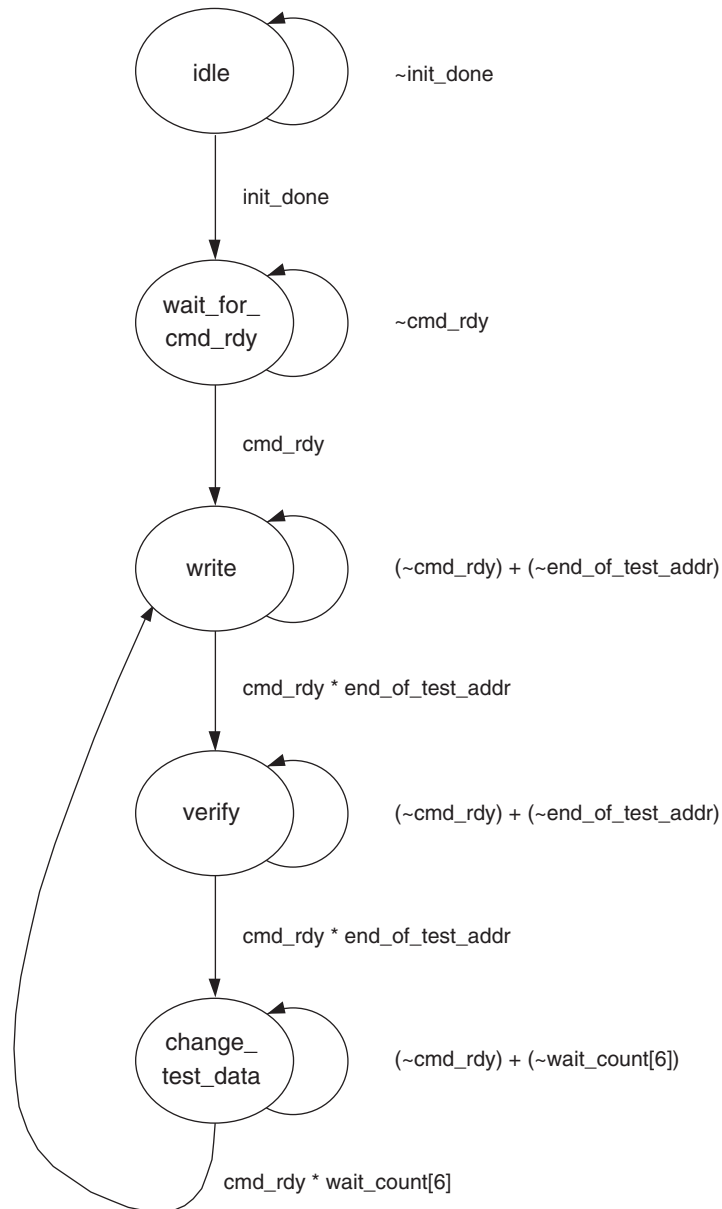
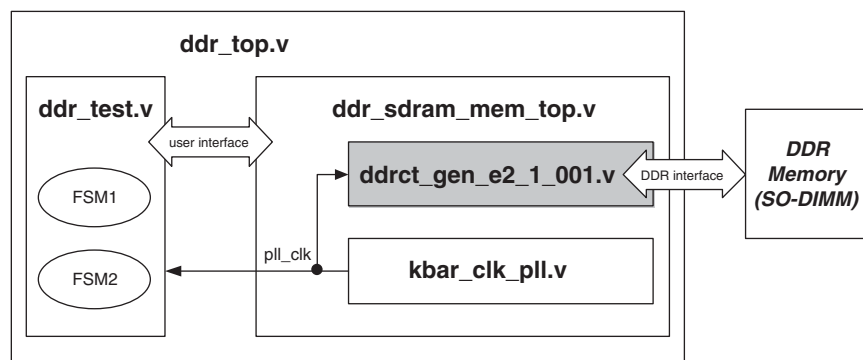
Test 3 started-----
Write to address 0x00000: 0x04 0xfb
Write to address 0x00004: 0x08 0xf7
Write to address 0x00008: 0x10 0xef
Write to address 0x0000c: 0x20 0xdf
Write to address 0x00010: 0x40 0xbf
Write to address 0x00014: 0x80 0x7f
Write to address 0x00018: 0x01 0xfe
Write to address 0x0001c: 0x02 0xfd
Write to address 0x00020: 0x04 0xfb
Write to address 0x00024: 0x08 0xf7
Write to address 0x00028: 0x10 0xef
Write to address 0x0002c: 0x20 0xdf
:
:
Write to address 0x7fff: 0x02 0xfd
Read from address 0x00000
Read from address 0x00004
:
:
Read from address 0x7fff

```

```

Test 3 started-----
Write to address 0x00000: 0xf7 0x08
:
:

```

Figure 1. FSM1 State Machine Diagram of the DDR Test Cycle**Figure 2. Block Diagram of the DDR Test Program**

Test Results

Two counters are implemented to show the number of successful and/or failed tests. The failure counter is increased by one when any data in any address location is incorrect. The success counter is increased only if all the data in all address locations are correct.

number_of_tests_passed: displayed on LEDs D8, D7, D6, D5

number_of_tests_failed: displayed on LEDs D4, D3, D2, D1

Waveform Measuring

For measuring write cycle timing, set a trigger at the falling edge of ball AC5 (signal cmd[0]) for the LatticeEC Advanced Evaluation Board and ball F2 (signal cmd[0]) for the LatticeXP Advanced Evaluation Board. For measuring read cycle timing, set a trigger at the rising edge of the same signal. The following images are DDR waveforms captured on the LatticeEC Advanced Evaluation Board using a Tektronix digital scope. The upper waveform is the DQS signal and the lower waveform is one of the DQ signals.

Figure 3. DDR Side Write Timing

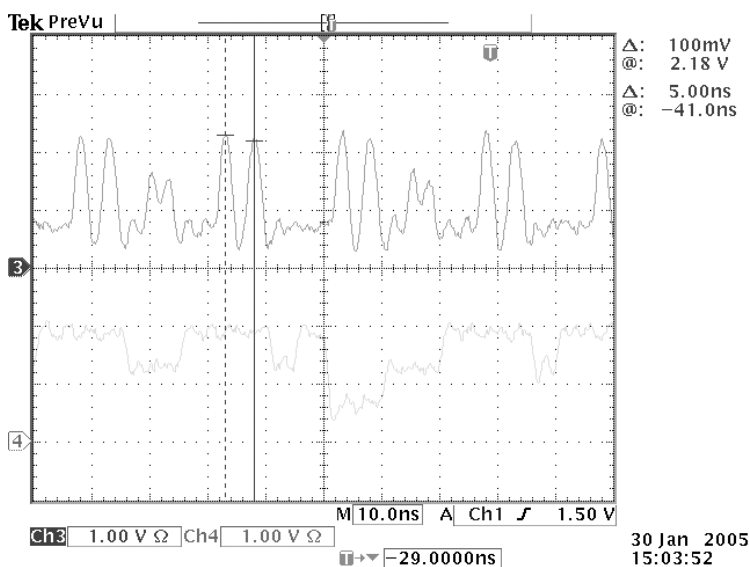


Figure 4. DDR Side Read Timing

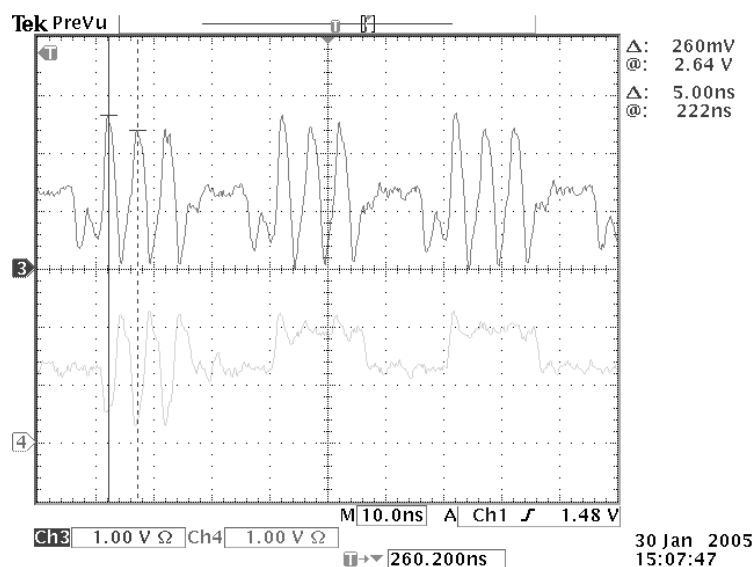
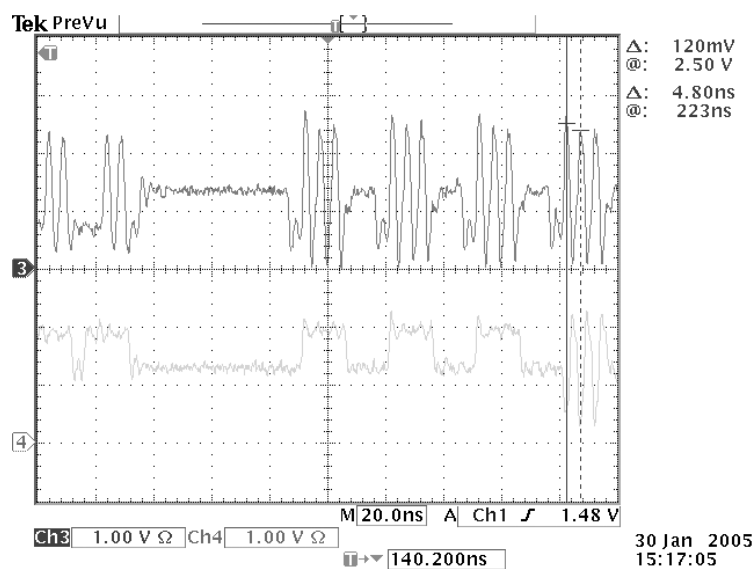


Figure 5. DDR Side Write to Read Timing



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Using the DDR Evaluation Bitstream with the LatticeEC and LatticeXP Advanced Evaluation Boards

The following images are user interface waveforms captured on the LatticeEC Advanced Evaluation Board using an Agilent logic analyzer.

Figure 6. User Side Write to Read Timing

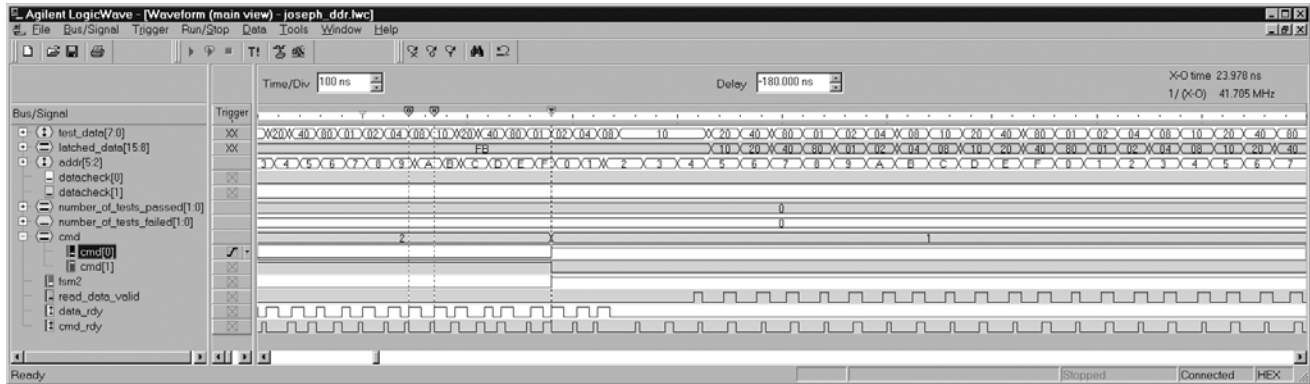


Figure 7. User Side Read to Write Timing

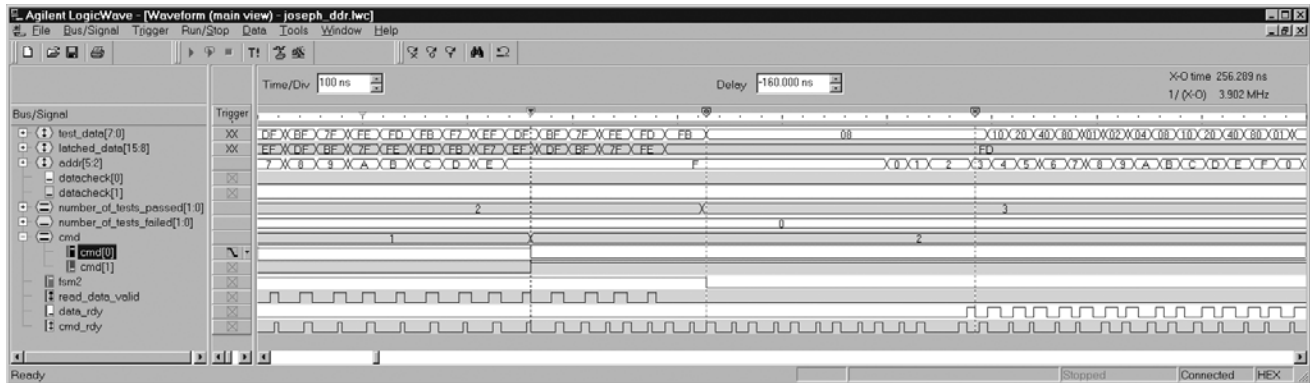
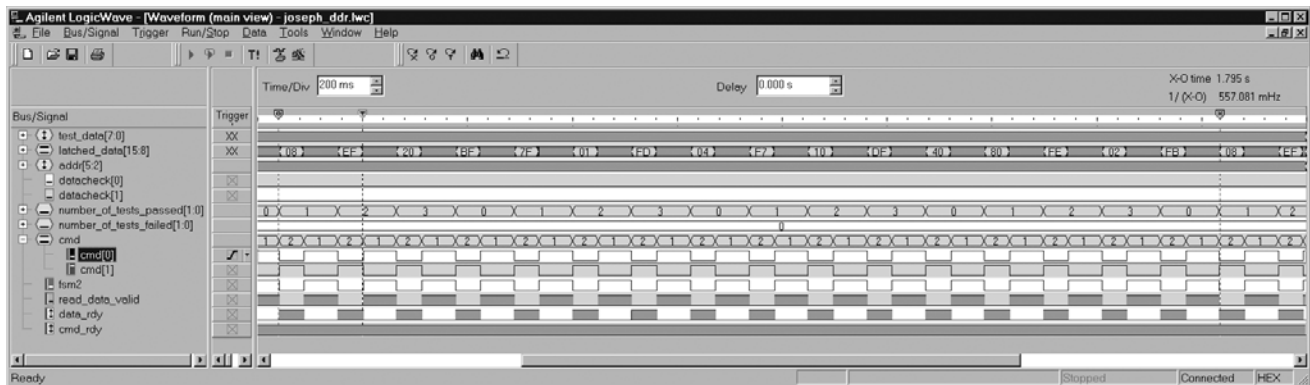


Figure 8. User Side Multiple Tests



Technical Support Assistance

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